Amendments to the Claims:

Please cancel, without prejudice, claims 6-9 and 14 as indicated below. This listing of claims will replace all prior versions and listing of claims in the application:

Listing of Claims:

1. (Previously Presented). A circuit for generating a reference current, comprising:

a positive feedback loop coupled with a floating current mirror, the floating mirror having a plurality of transistors;

a negative feedback loop diverting current from the floating current mirror;

wherein the circuit operates with a minimum supply voltage of approximately the sum of a transistor threshold voltage plus three drain saturation voltages;

wherein each source node of the plurality of transistors forming the floating current mirror are directly coupled together;

wherein the source node of each transistor forming the floating current mirror is not directly coupled to a ground node; and

wherein the source node of each transistor forming the floating current mirror is not directly coupled to a supply voltage node.

2. (Previously Presented) The circuit of claim 1, where the negative feedback loop diverts current directly from the floating current mirror.

3. (Previously Presented) The circuit of claim 1, where the negative feedback loop diverts current from the floating current mirror by using a voltage follower.

4. (Canceled)

5. (Previously Presented) The circuit of claim 1, wherein the floating current mirror comprises a floating MOSFET current mirror.

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Previously presented) A circuit providing a current reference, comprising:

a floating current mirror including a first transistor and a second transistor;

at least one resistor defining a voltage node;

a pull-down transistor coupled with the floating current mirror; and

an output transistor;

wherein the first transistor is coupled with the at least one resistor and provides an amount of current thereto;

wherein the second transistor is coupled with the output transistor for providing a bias signal to the output transistor;

wherein the amount of current provided by the first transistor into the at least one resistor is mirrored to the second transistor; and

wherein the pull-down transistor has one end coupled with the floating current mirror and a gate coupled with the voltage node, so as the amount of current provided by the first transistor increases, the pull-down transistor diverts an amount of current received by the first transistor.

12. (Canceled)

13. (Previously presented) The circuit of claim 11, wherein the amount of current mirrored to the second transistor provides a bias signal to the output transistor.

14. (Canceled)

15. (Previously presented) The circuit of claim 11, wherein the pull-down transistor is an n-channel MOSFET.

16. (Previously presented) The circuit of claim 11, wherein the output transistor is an n-channel MOSFET.

17. (Previously presented) The circuit of claim 11, further comprising:

a protection transistor coupled between the pull-down transistor and the floating current mirror.

18. (Previously presented) The circuit of claim 17, wherein the protection transistor is a p-channel MOSFET.

19. (Previously presented) The circuit of claim 11, wherein a load is coupled to the output transistor, the load receiving the current reference.

20. (Previously presented) The circuit of claim 11, wherein the first and second transistors are p-channel MOSFETS.

21. (Previously Presented) The circuit of claim 5, wherein the floating MOSFET current mirror includes a pair of p-channel transistors.

22. (Previously presented) The circuit of claim 11, wherein the pull-down transistor is coupled with the floating current mirror through a MOSFET transistor.